CLAIMS

We claim:

1. A programmable logic device comprising:

a system bus;

a plurality of configuration memory cells; and

a memory interface, coupled to at least one of the configuration memory cells and couplable to the system bus via a programmable interconnect, adapted to provide access to the at least one configuration memory cell after configuration of the programmable logic device to write data carried by the system bus to the at least one configuration memory cell.

2. The programmable logic device of Claim 1, further comprising a system bus register file, coupled to the system bus and couplable to the programmable interconnect, adapted to provide an interface between the memory interface and the system bus.

3. The programmable logic device of Claim 2, wherein the system bus register file is adapted to communicate with a plurality of the memory interfaces.

4. The programmable logic device of Claim 1, wherein the at least one configuration memory cell is associated with a special functional block within the programmable logic device.

5. The programmable logic device of Claim 4, wherein the special functional block comprises a phase-locked loop circuit, a delay-locked loop circuit, an input/output circuit, and/or a memory interface controller.

6. The programmable logic device of Claim 1, wherein the configuration memory cells comprise static random access memory cells and/or flip flops.

7. The programmable logic device of Claim 1, wherein the memory interface communicates with the at least one configuration memory cell in byte increments.

8. The programmable logic device of Claim 1, wherein a programmable identification number is associated with the memory interface.

9. The programmable logic device of Claim 8, wherein the programmable identification number is set via one or more of the configuration memory cells.

10. The programmable logic device of Claim 8, further comprising at least one additional memory interface, wherein the memory interfaces may have the same programmable identification number.

11. A programmable logic device comprising:

a system bus;

a programmable interconnect;

means for storing configuration data; and

means for interfacing with the storing means after configuration has completed to change the configuration data stored by the storing means with data carried by the system bus, wherein the interfacing means is couplable to the system bus via the programmable interconnect.

12. The programmable logic device of Claim 11, wherein the interfacing means is addressed via one or more programmable identification numbers.

13. The programmable logic device of Claim 11, wherein the storing means comprises static random access memory cells.

14. The programmable logic device of Claim 11, further comprising a system bus register file adapted to couple to the programmable interconnect and interface the system bus to the interface means.

15. The programmable logic device of Claim 11, wherein the storing means is associated with a special functional block.

16. A method of modifying configuration data stored within a programmable logic device after configuration has been completed, the method comprising:

providing memory interfaces for a plurality of configuration memory cells which store at least a portion of the configuration data;

providing a system bus for carrying data to be written to at least some of the plurality of the configuration memory cells; and

providing a programmable interconnect adapted to couple the system bus to the memory interface to route the data from the system bus to the memory interface.

17. The method of Claim 16, wherein each of the memory interfaces is addressed via an associated programmable identification number.

18. The method of Claim 17, wherein the programmable identification number may be the same for one or more of the memory interfaces.

19. The method of Claim 16, wherein the plurality of the configuration memory cells are associated with special functional blocks.

20. The method of Claim 16, further comprising providing a system bus register file to interface the system bus to each of the memory interfaces via the programmable interconnect.